

EtherCAT[®] Master Stack Technical Presentation

EC Master

Features according to ETG.1500 Master Classes



Master Core Features (1)



Feature name	Master Class A	Master Class B					
Basic Features							
Service Commands, IRQ field in datagram, Slaves with Device Emulation, EtherCAT State Machine, Error Handling, EtherCAT Frame Types	✓						
Sophisticated error detection and diagnosis: Lost cable connection, missing/wrong, slave response, slave operation monitoring, Ethernet link layer debug messages, > 200 error codes	·						
VLAN	✓						
Process Data Exchange							
Cyclic PDO (High performance up to 50 us cycle time), Multiple Tasks	√	•					
Network Configuration							
Online scanning, Reading ENI, Compare Network configuration, Explicit Device identification, Station Alias Addressing, Read and Write to EEPROM	✓						



Master Core Features (2)



Feature name	Master	Master
Mailbox Support	Class A	
State change check: Logical and physical polling		✓
Resilient Layer (repeating mailbox communication)	✓	✓
Multiple mailbox channels (multiple protocols in parallel)	✓	✓
CoE Mailbox Protocol		
SDO Up- and Download,		✓
Normal, Expedited and Segmented Transfer,		
SDO Info service (Read Object Dictionary),		
Complete Access, Emergency Message		
EoE Mailbox Protocol		
Services for tunneling Ethernet frames. includes all	✓	✓
specified EoE services Virtual Switch		
EoE Endpoint interface to Operating Systems	FP	
FoE Mailbox Protocol		
FoE Services	✓	
Firmware Up- and Download	 ✓ 	
Boot State	✓	



Master Core Features (3)



Feature name	Master	Master Class B
SoE Mailbox Protocol		
SoE Services	✓	 ✓
AoE Mailbox Protocol		
AoE Services	✓	
VoE Mailbox Protocol		
VoE Services	✓	
Synchronization with Distributed Clock (DC)	E.	
Initial propagation delay measurement,	✓	
Offset compensation, Set start time,		
Continuous drift compensation,		
Sync window monitoring		
Master must synchronize itself on the reference clock.	✓	
DC master synchronization (DCM).		
Slave-to-Slave Communication		
via Master, required for safety devices	✓	✓



EC Master

EtherCAT Network Timing

Interaction between application and EtherCAT network traffic



EtherCAT Master and application on a single CPU





Classic solution with cpu-powered fieldbus card:

→ Fieldbus software and application tasks running on different CPUs

ightarrow Real-Time is guaranteed by fieldbus card

EtherCAT Master as software solution:

 \rightarrow No extra CPU required. EC-Master consumes low CPU time.

- ightarrow Master is integrated in control loop
- → Real-Time OS or Real-Time Extension required for application and EtherCAT Master



EC *Master*

EC-Master without internal tasks



EtherCAT Master has no internal tasks:

From the application side it looks like a driver, which is activated by calling some simple functions (Read, Write, Admin).

- Benefits:
- No synchronization issues between application and EtherCAT Master.
- Consistent process data without using any locks.
- The application decides, what shall be done at which time
- Cyclic part may run within Interrupt Service Routine (ISR)
- Easy to integrate



Cyclic jobs



1	EtherCAT Master: Refresh Inputs
Ο	EtherCAT Master: Write Outputs eUsrJob_SendAllCycFrames: Send cyclic frames
МТ	EtherCAT Master: Administration eUsrJob_MasterTimer: Trigger master and slave state machines
AS	EtherCAT Master: Send acyclic datagrams/commands eUsrJob_SendAcycFrames: Transmit pending acyclic frame(s).
Арр	Application: Work on inputs and create output values



Cyclic and acyclic EtherCAT frames



- Cyclic frames:
 - Contain process output and input data
 - Distributed Clocks (DC): Contain datagram to distribute network time
 - Typically sent by master in every cycle
 - Defined by the configuration tool (which data to read and to write)

• Acyclic frames:

- Asynchronous, event triggered communication
- Mailbox communication (CoE, FoE, EoE)
- Status requests (e. g. read slave state information)
- Raw EtherCAT datagrams requested by application



Network Timing: Cyclic frames <u>No</u> interrupt from network controller





hnologies

Network Timing: Cyclic and acyclic frames <u>No</u> interrupt from network controller





hnologies

V1.7

Feature Pack: Split Frame Processing



- Split I/O data processing into several application tasks
- Split processing of acyclic communication into a separate task



Feature Pack: Split Frame Processing Network Timing: Split cyclic frame processing





Feature Pack: Split Frame Processing Network Timing: Split cyclic and acyclic frame processing

EC
Master





EC Master

EtherCAT Synchronization



Network Timing: Cyclic Frames with DC Sync Signals <u>No</u> interrupt from network controller





chnologies

Distributed Clocks Master Synchronization





EC ← Master

Bus Shift Mode Reference Clock controlled by Master/Controller Time



Bus Shift: DC Reference Clock follows the Master Clock/Timer

- Adjust the Bus Time Register of the DC Reference Clock.
- The DC slaves converge to this time.
- Frame send time used for drift measurement (time is related to master timer)



EC *Master*

Master Shift Mode Master/Controller Time controlled by Reference Clock



Master Shift: Master Clock/Timer follows the DC Reference Clock

- The timer (reload value) on Master control system (Host) is adjusted.
- E. g., if the Host is to fast, increase the reload value for one tick and then switch back to the default value.
- Interface to adjust timer required. Not available on all operating systems!



Distributed Clocks Master Sync DCM Mode Selection Criteria



Criteria	Bus Shift Mode	Master Shift Mode
Accuracy of SYNC Signals	+/- 1000 nanosec jitter	+/- 20 nanosec jitter
Maximum acceptable drift between master and reference clock	600 ppm → very precise timer in control system required	no physical limitation
Multiple EtherCAT networks	possible	not possible
Implementation	possible	not possible on all operating systems



Network Timing: Sync Manager (SM) Synchronization <u>With Interrupt from network controller</u>



Inologies

EC
Master

Network Timing: Sync Manager (SM) Synchronization



- Alternative synchronization instead of using DC, much simpler to implement
- Drawback: slave delay time not compensated
- Drawback: slave timing related to master frame send time jitter
 - minimum send time jitter is required
 - send frames immediately after timer irq on master
- Immediate slave reaction on new data (update when frame is received)



Feature Pack: External Synchronization (1)



The external synchronization feature pack allows the synchronization of two or more EtherCAT segments by a Bridge device, e. g. Beckhoff EL6695



The synchronization process is divided in two parts; DCM and DCX.

- DCM: Synchronize Master timer to slave. (MasterShift)
- DCX: Synchronize slaves to bridge device. (BusShift)



Feature Pack: External Synchronization (2)



- The Bridge has two EtherCAT connections. The primary port is connected to the primary segment; the secondary port is connected to the secondary segment. The Bridge provides an internal (primary port) and an external (secondary port) time stamp which is used by the Master to adjust the Ref-Clock.
- The Bridge device must support the "External Synchronization Status" PDO 0x10F4 see document ETG.1020 chapter "21.1.2 Synchronization by a Bridge device".
- During startup the two segments can be powered-on at different times. That means that there will be an absolute time difference between the two segments.



EC Master

EtherCAT[®] over Ethernet (EoE)



Class A: Includes Virtual Ethernet Switch for EoE







Class A: Includes Virtual Ethernet Switch for EoE







Configure drives connected to the EtherCAT network without additional cables

Windows Network Driver for EoE Endpoint with RAS

Windows Network Driver for EoE Endpoint with RAS

V1.7

40

EoE TAP Network Driver (Windows)

Nicht identifiziertes Netzwe... TAP-Windows Adapter V9

			1	
Netzwerkverbindungsdetai	ls	×		
Netzwerkverbindungs <u>d</u> etails:				
Eigenschaft Verbindungsspezifisches Beschreibung Physische Adresse DHCP-aktiviert IPv4-Adresse IPv4-Subnetzmaske IPv4-Subnetzmaske IPv4-Standardgateway IPv4-DNS-Server IPv4-WINS-Server NetBIOS über TCPIP ak	Wert TAP-Windows Adapter V9 00-FF-D4-8C-AA-FC Nein 192.168.150.1 255.255.255.0 Ja			
Verbindungslokale IPV6 IPv6-Standardgateway IPv6-DNS-Server	fec0:0:0:ffff::1%1 fec0:0:0:ffff::2%1 fec0:0:0:ffff::3%1 <u>Schließe</u>	n		IP-Address 192.168.150.1

EC-EoE-Gateway

C-EoE-Gateway V2.9.2 Status Please select a netwo enter the IP Address o	2.05 ork adapter, of the running master unit and press start.	×
Status Please select a netwo enter the IP Address o	ork adapter, of the running master unit and press start.	
Please select a netwo enter the IP Address o	ork adapter, of the running master unit and press start.	
EoE Network Settings	3	
TAP Adapter:	EoE (TAP-Windows Adapter V9)	~
IP Address:	192.168.150.1	
		IP-Address
RAS Connection Setti	ings	192.168.15
Requires running RAS	Server	
Master IP Address:	127.0.0.1	
Port:	6000	
Master Instance:	0	
Run gateway auton	Stop Save Cl	ose
		.:

- Select TAP adapter used
- Select Master to connect to
- Start
 - EoE Gateway connects to remote master and enables the TAP adapter
 - IP-connection to remote system is available
 - Any tool can then use slave devices which support EoE

Setting IP address in EC-Engineer

A EC-Engineer []			- 🗆 X
<u>F</u> ile <u>V</u> iew <u>N</u> etwork <u>S</u> ettings <u>H</u> elp			
Configuration Mode Report ENI	📕 Diagnosis Mode		÷
Project Explorer	Device Editor		
 Ulass-A Master 	General PDO Mapping Variables	Ethernet Advanced Options Distributed Clo	ock Init Commands CoE Obj 🕨
1001 [SGD7S-xxxxA0x CoE Drive]	(10) Ethernet	V	
	Virtual MAC address	02 00 00 00 03 E9 🖌 Auto	102 168 1E0
	re Stamp Requested		192.108.150.
	Port Mode	○ Switch Port	
	Overwrite IP Settings	\checkmark	
Slave supports EoE	IP Address	192 . 168 . 150 . 5	
	Subnet Mask	255 , 255 , 255 , 0	
	Default Gateway	1 0 0 0	
	DNS Server	1 0 0 0	
	DNG Nerre	1.0.0.0	
	DNS Name		
<	>		
Cl. : M. Elat View Tanalam View			
Classic View Plat View Topology View			
Short Info 🔹 🔻	* Messages		▼ *
Information	Severity Time Message		
Name Slave_1001 [SGD7S-xxxxA0x C	0		
Description SGD7S-xxxxA0x EtherCAT(CoE			
Vendor Yaskawa Electric Corporation (0		
Naturalus 1 Slavas 1			
etworks: 1 blaves: 1		5	tate: I Mode: CONFIG EXPERT

EC Master

Performance Measurements

7 Slaves: EK1100 + 2xEL2004 + 2xEL1004 + EL4132 + EK1110

Load: One cyclic frame (Size=579 Bytes) with 512 Bytes Process Data and mailbox transfer to EL4132

		x86: Intel Atom 1600 MHz NIC: Realtek 8111 Windows CE 6.0		TI Sitara 720 NIC: In witho	AM3359 MHz iternal ut OS	PowerP(1200 NIC: R 81 VxW	C e500v2 MHz ealtek 11 orks
Nr	EC-Master Funktion	Avg µsec	Max µsec	Avg µsec	Max µsec	Avg µsec	Max µsec
1	Process Inputs	2.4	7.2	8.7	20.5	5.1	7.8
2	Send Outputs	5.2	7.6	6.1	9.3	6.3	7.5
3	Administration	5.5	24.9	3.3	15.7	3.7	7.3
4	Send Acyclic Frame	0.9	4.4	0.6	8.0	1.1	5.1
	Total CPU Time	14.0	44.1	18.7	53.5	16.2	27.7

Round-Trip Time on different systems

- 7 Slaves: EK1100 + 2xEL2004 + 2xEL1004 + EL4132 + EK1110
- Load: One cyclic frame (Size=579 Bytes) with 512 Bytes Process Data and mailbox transfer to EL4132

		x86: Intel Atom 1100 MHz NIC: Realtek 8111 Windows CE 6.0		x86: Cor 2400 NIC: Intel IntervalZ	e2Quad MHz Pro/1000 ero RTX	PowerP0 1200 NIC: Rea VxW	C e500v2 MHz Itek 8111 orks
Nr	EC-Master Funktion	Avg µsec	Max µsec	Avg µsec	Max µsec	Avg µsec	Max µsec
1	Round-Trip (Out+Inp)	94.4	112.2	67.0	82.1	74.6	88.1
2	Administration	7.0	10.2	0.8	2.5	3.1	4.7
3	Send Acyclic Frame	1.5	6.4	1.1	3.6	1.1	5.1

CPU load depending on number of slaves

Device: IXXAT Econ 100, **CPU:** Xilinx Zynq SoC - Dual-Core Cortex-A9, 666 MHz

Software: Linux with EC-Master V2.6.2, Link Layer GEM

Cortex [™] -	A9 Sight [™] I	Multico	re Debug	and T	race	
ARMv7 32b CPU						
16-64k I-Cache	16- D-C	64k ache	Core 1	2	3	4
ACP				scu		
Dual 64-bit AMBA3 AXI						

EC Master

Number of Slaves	16	32	64
Network cycle time	250 usec	500 usec	1000 usec
Payload	128 Bytes	256 Bytes	512 Bytes
EC-Master Function			
Process Inputs [usec]	33.7	34.1	36.1
Send Outputs [usec]	17.0	17.9	18.8
Administration [usec]	13.8	21.0	49.4
Send Acyclic Frame [usec]	13.6	15.4	15.6
Total Time [usec]	78.1	88.4	119.9
CPU Load [percent]	31 %	18 %	12 %

EC Master

Quality Assurance Success Stories

High Quality - Software Quality Assurance

- Source code management software, Configuration Management
- Automatic build process for all supported operating systems
- Well defined release process with regression tests
- Deep knowledge in various real-time OS
- Long term experience with real-time systems
- Acceptance test with integrated frame loss simulation
- Acceptance test with many different EtherCAT slaves
- EtherCAT conformance assurance
 - Attendance in all ETG Technical Committee Meetings
 - Plug Fests
 - Active, Leading Member in several ETG Working Groups (e.g. EAP)
 - Very good and close contacts to ETG, Beckhoff and Hilscher

Test Equipment - I/O

Master systems:

- Different operating systems
- Different CPU architectures
- Different performance classes

Slaves:

- Various manufacturers
- Digital/analog I/O
- Drives (Copley, Omron, Yaskawa, etc.)
- Safety (FSoE) devices
- In total >400 slaves (not just in these racks)

Test Equipment - Distributed Clocks

EC Master

EtherCAT[®] and GPL

EC-Master on Linux

EtherCAT[®] Licensing

What is necessary to use EtherCAT?

- Member of the EtherCAT Technology Group (ETG)
- Recommended: Beckhoff "ETHERCAT MASTER LICENSE AGREEMENT"
- Whereas, Licensor is the owner of all intellectual property rights pertaining to the EtherCAT Technology, including but not limited to (a) the following German patent applications and patents: EP1590927, EP1789857, DE102004044764, DE102007017835 with corresponding applications or registrations in various other countries, and (b) the trademarks "EtherCAT" and "Safety over EtherCAT", with applications or registrations in the European Community (CTM003122736, CTM006350029, CTM005460563) and corresponding registrations or applications in various other countries.
- Whereas, Licensee intends to create and/or sell or otherwise distribute a product incorporating the EtherCAT Technology;
- Whereas, Licensor is willing to permit Licensee to create and/or sell or otherwise distribute a product incorporating the EtherCAT Technology;
- Whereas, Licensee acknowledges Licensor's commercially reasonable efforts to keep the number of those EtherCAT Technology products in the market sold under the trade name "EtherCAT" and not being fully compatible with the then current version of the EtherCAT Technology at a minimum.

Linux and the GNU General Public License (GPL)

 The GPL is the first copyleft license for general use, which means that derived works can only be distributed under the same license terms.

• GPL:

6. Each time you redistribute the Program (or any work based on the Program), the recipient automatically receives a license from the original licensor to copy, distribute or modify the Program subject to these terms and conditions. <u>You may not impose any further restrictions</u> on the recipients' exercise of the rights granted herein. You are not responsible for enforcing compliance by third parties to this License. http://www.gnu.org/licenses/gpl-2.0.html

 The Linux kernel is released under the GNU General Public License version 2.

ETG web site: <u>http://www.ethercat.org/en/faq.html#790</u>

3.4 How about Open Source? EtherCAT technology itself is not Open Source. → EtherCAT cannot be licensed in conjunction with ANY Open Source License!

Backed by the standardization of EtherCAT by IEC, ISO and SEMI, access to EtherCAT technology is available to everyone to non-discriminatory terms. Additionally, Master Licenses are free of royalties. Maintenance and all further development of the technology is available to all users by membership within the ETG, the user group for EtherCAT technology. If you have questions regarding implementing or using EtherCAT in conjunction with shared source or open source systems please contact ETG headquarters or Beckhoff, the EtherCAT technology licensor.

EC-Master Architecture on Linux

EC
Master